



GPLB5X Development Board User Manual v0.1

January 28, 2008

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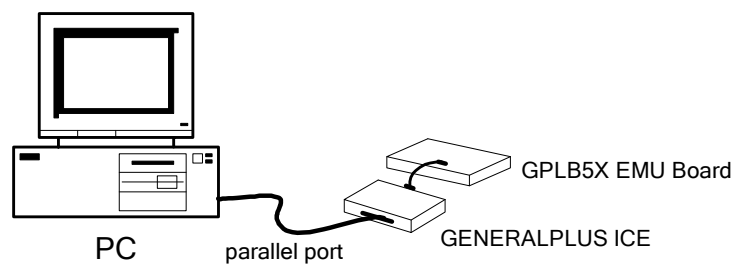
1 REVISION HISTORY

Revision	Date	By	Remark
V0.1	Jan,28, 2008	Scott	Original

2 INTRODUCTION

2.1 Hardware Architecture

The GPLB5X EMU Board is a shared board for GPLB52001A and GPLB52640A. Programmer can easily emulate these devices on board. Simply apply the following connection to start developing your project. Make sure power is properly supplied to both ICE and EMU board.



A hardware overview of GPLB3X development system

2.2 GPLB5X Development component list

Hardware

1. GPLB5X EMU board
2. Parallel connector (connects ICE & GPLB5X EMU board)
3. GENERALPLUS ICE (In-Circuit Emulator; sold separately)
4. Parallel port (connects to your personal computer; not included in the development kit)
5. Power supplier or adapter with 5V output (not included in the development kit).

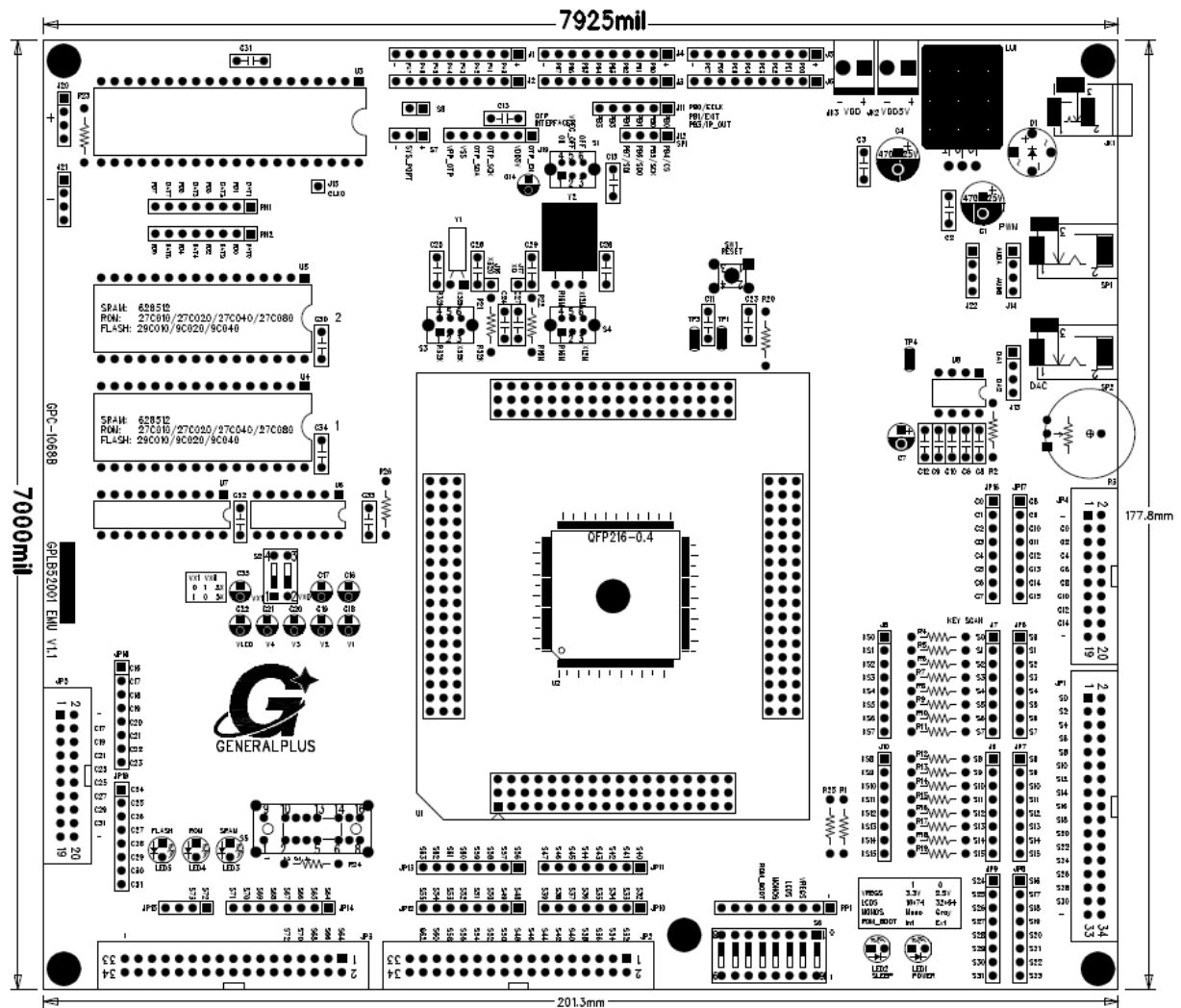
Software

1. FortisIDE software tool. (Please use version 3.0)

3 EMU BOARD

3.1 GPLB5X EMU Board v1.1

EMU chip: GPLB52001



Settings Description

S1: VREG_OFF switch

Name	ON	OFF	Function
VREG_OFF	Enable Power Regulator	Enable Power Regulator	LCD Charge Pump control

S2: Fixed and Don't change.

S3: 32768Hz selector

Name	VCC	GND	Function
32768Hz Select	R32K	X32K	32768Hz source select

S4: System clock selector

Name	VCC	GND	Function
Sys_CLK	X12M (12MHz X'TAL)	X16M (ROSC)	System Clock Select

S5: Memory Selector (SRAM/ROM/FLASH)

LED3: SRAM LED

LED4: ROM LED

LED5: FLASH LED

S6:

SW Number	Name	SHORT	OPEN	Description
1	--			N/A
2	VREGS	3.3V	2.6V	Power Regulator Selector
3	LCDS	16 x 74	32 x 64	LCD dot size selector
4	MONOS	MONO	GRAY	LCD display mode selector
5	ROM_BOOT	INTERNAL	EXTERNAL	ROM Boot
6	--			N/A
7	--			N/A
8	--			N/A

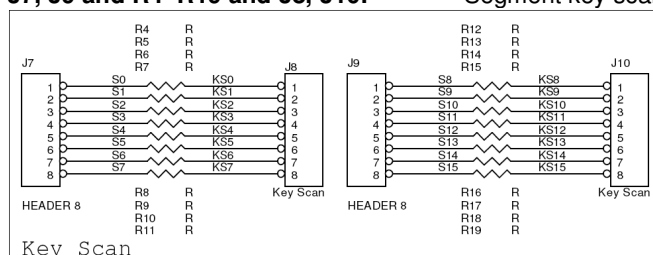
S7: OPEN

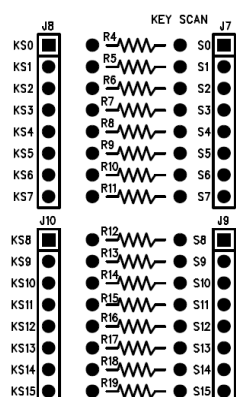
S8: Fixed and Don't change.

SW1: RESET Switch

JP1~JP19: Common and segment socket

J7, J9 and R4~R19 and J8, J10: Segment key scan output





J1, J2: PortA

J2, J4: PortB

J5, J6: PortC

J11: ECLK, EXTI, IR Output connector

J12: SPI interface

JK1: Adapter input (9V)

JK2: General power input (5V)

J20: General power input (5V)

JK3: 3V VDD power Input

J21: GND connector

LED1 : Power LED (ON when powered on)

LED2: Sleep LED (ON while sleeping)

LED3 : RAM LED (ON when switch S5 to RAM)

LED4 : ROM LED (ON when switch S5 to ROM)

LED5: FLASH LED (ON when switch S5 to FLASH)

LED5 : DAC MONO LED(ON when Audio outputs are Dac mono)

LED6 : DAC STEREO LED(ON when Audio outputs are Dac stereo)

LED7 : PWM LED (ON when Audio outputs are PWM outputs)

R22: System clock resistor (ROSC)

R21: R32K resistor

Y2: 12MHz X'TAL for System Clock

Y1: 32768Hz X'TAL

U1, U2: GPLB52001 Chip

U3: CPU socket for ICE used

U4,U5: RAM / ROM / FLASH, dependent on S5

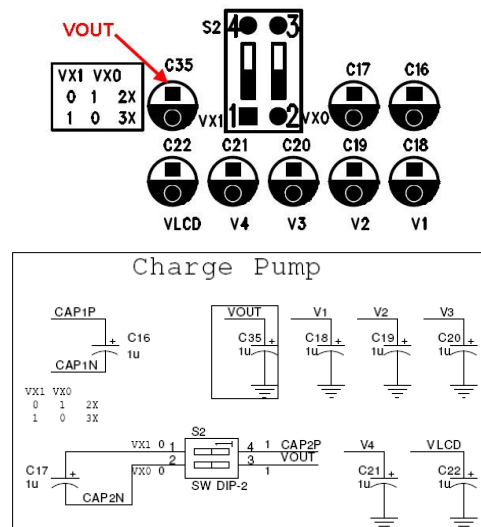
U8: GPY0030 OP-AMP

SP1: PWM outputs speaker
J14, J15: PWM output connector

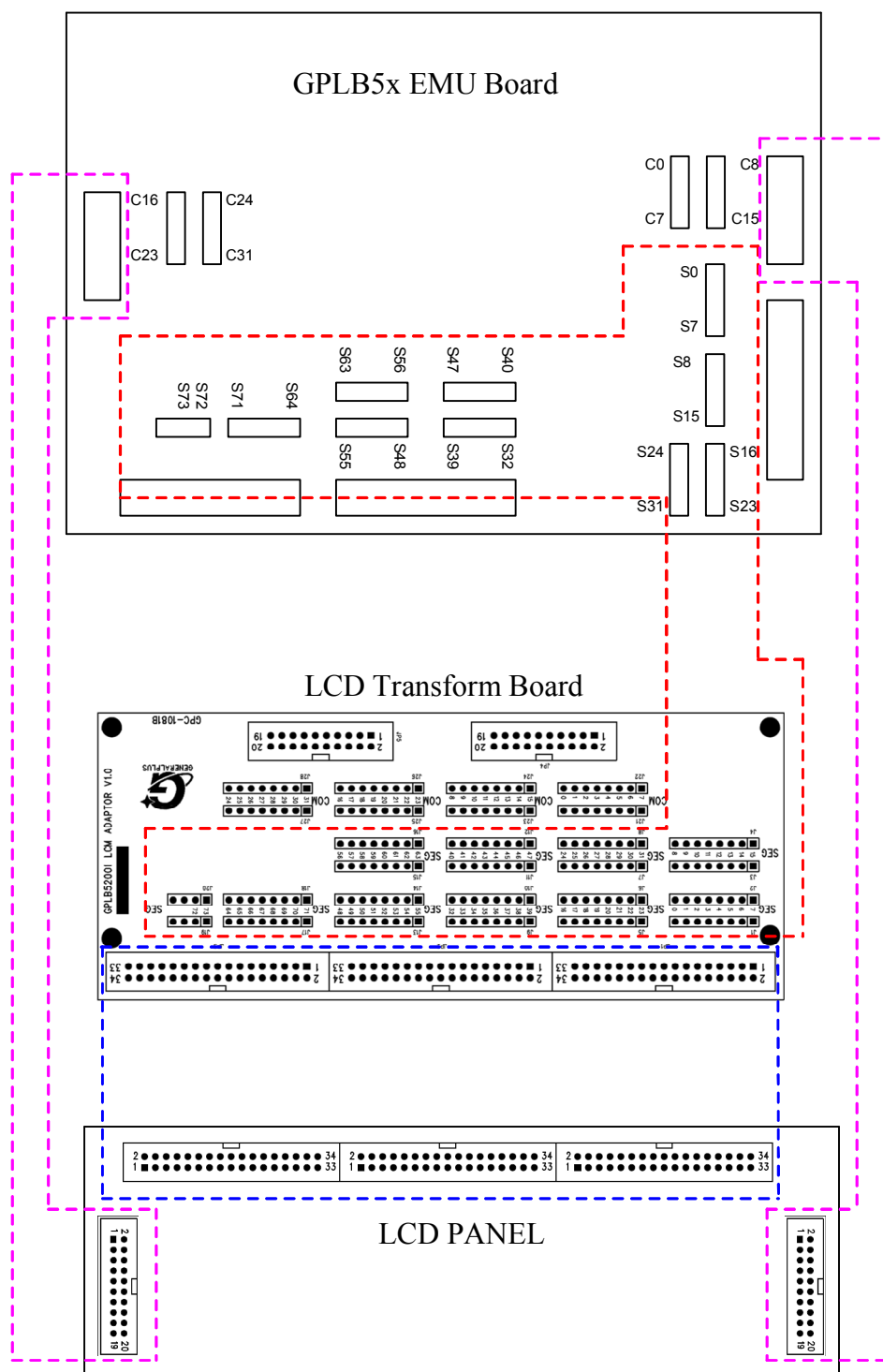
SP2: DAC output Speaker
J13: DAC output connector

Problems found in the 1st version GPLB52001: (estimated schedule of 2nd version GPL52001 is Mar/2008 ready, All 1st version boards need to be replaced by 2nd version boards then)

1. VLCD is not stable in this GPLB52001 1st version, and GENERALPLUS can fix it in next version. If user wants to connect to LCD panel, It needs addition **8V power supply on VOUT pin** of GPLB52001.



2. When GPLB52001 is selected to the mode of **4 Gray level**, 32 COM x 64 SEG, the SEG60~SEG63 can not display correctly, SEG48~SEG51 data will be displayed on both SEG48~SEG51 and SEG60~SEG63. When GPLB52001 is selected to the mode of **4 Gray level**, 16 COM x 74 SEG, the SEG70~73 can not display correctly, SEG58~SEG61 data will be displayed on both SEG58~SEG61 and SEG70~SEG73. But when GPLB52001 is selected to **Black and White** mode, no matter 32 COM x 64 SEG or 16 COM x 74 SEG mode, it is OK, no problem.
3. This 1st version GPLB52001 EV board need to connect to a transform board to fix the wrong SEG sequence problem. Please see following diagram. It will be fixed in the 2nd version.



4 APPENDIX A: GPLB5X EMU BOARD SCHEMATICS

